REMARKS/ARGUMENTS

Claims 27-35 are canceled above. Claims 36-41 remain pending. Claims 36, 37, 39 and 41 are amended to clarify their respective languages and more fully define the scope of the inventions recited therein. The amendments to independent claim 36 is supported by the exemplary embodiment of the input/output cell shown in Figure 7 as well as its corresponding description in the original disclosure. The amendments to independent claim 39 is supported by the exemplary embodiment of the input/output cell shown in Figure 8 as well as its corresponding description in the original disclosure.

Claims 36-38 and 41 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Miyanaga et al. (USP 5,514,893, hereinafter Miyanaga) in view of Toyoshima (US 200100177555, hereinafter Toyoshima), Lin (USP 6552594, hereinafter Lin) and Fugate et al. (USP 6525549, hereinafter Lin). Applicants respectfully traverse these rejections for at least the following reasons.

In rejecting claim 36, the Examiner asserts:

"Miyanaga et al's Figure 1 shows an integrated circuit comprising: a pull-up MOS transistor (4) coupled between a first supply voltage and a pad; a pull-down MOS transistor (5) coupled between the pad and a second supply voltage that is lower than the first supply voltage; an active diode (2) having a second terminal coupled to the pad. "

Applicants respectfully traverse these rejections for at least the following reasons. In Miyanaga, diode 2 is connected between the pad and the supply voltage. In contrast, in claim 1, one terminal of the diode is connected to the pad, and the other terminal of the diode is connected to the drain terminal of the first MOS transistor, as shown in the exemplary embodiment of Figure 7 of the present application.

As pointed out correctly by the Examiner, Miyanaga fails to show, among other elements, a first MOS "transistor coupled between the diode and the first supply voltage." The Examiner thus points to Fig 2 of Toyoshima and asserts: "Toyoshima's figure 2 shows diode D1

and switch F1 are coupled between pad 10 and Vcc in order to provide a controllable clamp circuit".

Applicants submit that contrary to the Examiner's assertions, elements F1 and F2 shown in Figure 2 of Toyoshima are fuses and not switches or transistors:

"Specifically, FIG. 2 shows the construction of the input protection device formed inside the LSI according to the first embodiment of the present invention. As shown in FIG. 2, an internal element of the integrated circuit, i.e., a MOS gate included in a MOS gate input circuit 11, is connected to a signal input terminal 10. A series circuit consisting of a first diode D_1 for the input protection and a first fuse element F_1 is connected to a node in an input signal path formed between the signal input terminal 10 and the MOS gate such that one terminal of the first fuse element F_1 is connected to the node, the other terminal of the first fuse element F1 is connected to the anode of the first diode D_1 and the cathode of the first diode D_1 is connected to a first voltage supply node (Vcc voltage supply line). The first diode D_1 is, therefore, connected in reverse polarity between the Vcc voltage supply line and the signal input terminal 10 via the first fuse element F_1." (paragraph 32)

Furthermore, fuse F1 of Figure 2 of Toyoshima is coupled between the pad and diode D1. In contrast, claim 1 requires that none of the terminals of the "first MOS transistor" be coupled to the input/output pad. Moreover, diode D1 of Figure 2 of Toyoshima is coupled between the fuse and the supply voltage. In contrast, in claim 1, the diode is coupled between the pad and the drain terminal of the first MOS transistor. Miyanaga, whether taken alone, or in combination with Toyoshima, Lin and Fugate fails to teach or suggest claim 36.

In rejecting claim 36, the Examiner further states:

"Lin's figures 11a and figures 11b show the function of the diode in circuit 60 will not be changed when the positions of switch P1 and the diode are exchange. Therefore, it would have been obvious to one having ordinary skill in the art to add a PMOS switch (i.e. Lin's

transistor P1) connected between Miyanaga's diode 2 and the first supply voltage for the purpose of having more flexibility of enabling/disabling the clamp diode 2."

Applicants disagree. A person of ordinary skill in the art would see no reason to combine Lin with Miyanaga and thus would not be motivated to do so in the manner suggested by the Examiner. The Examiner asserts that by adding a PMOS switch (i.e. Lin's transistor P1) between Miyanaga's diode 2 and the first supply voltage "more flexibility of enabling/disabling the clamp diode 2" is achieved. However, there is no motivation to modify Figure 1 of Miyanaga to add this alleged "flexibility" since, as best understood, there does not appear to be any reason to clamp diode 2 of Miyanaga. If the Examiner believes otherwise, he/she is requested to explain with specificity his/her reasoning for this assertion. Furthermore, as recited in claim 36, the bulk terminal of the first MOS transistor receives the higher of the pad voltage and the first supply voltage. In contrast, the bulk terminal of transistor P1 of Lin appears to be connected to a fixed voltage.

In rejecting claim 36, the Examiner further states:

"The modified Miyanaga et al.'s figure 1 further fails to show "a biasing circuit adapted to apply to bulk regions of the pull-up MOS transistor and the first MOS transistor switch the higher of a voltage applied to the pad and the first supply voltage". However, Fugate et al.'s 2 teaches that a bulk of PMOS transistor is selectively coupled to the highest voltage in order to prevent sudden voltage drop at the bulk, thereby reducing output noise. Therefore, it would have been obvious to one having ordinary skill in the art to use Fugate et al.'s bias circuit to bias the bulks of the pull-up MOS transistor (4) and the added PMOS switch in order to reduce output noise and power consumption."

Applicants respectfully disagree for at least the following reasons. Fugate is directed to a power amplifier and not to an input/output cell. Furthermore, there is no motivation to combine Fugate with Miyanaga and Lin. The Examiner's assertion that Fugate's bias circuit when applied to "bias the bulks of the pull-up MOS transistor (4) and the added PMOS switch"

reduces output noise and power consumption is erroneous and misses the point as to why claim 36 requires a hot-socket circuit. The hot-socket circuit ensures that the drain-to-well (bulk) regions of the pull-up and first MOS transistors are not inadvertently forward, thus preventing current conduction between these two regions, as described on page 15, lines 18-21 of the present application and reproduced below for the Examiner's convenience:

"[0078] The hot-socket circuit 735 tracks the higher voltage between the supply VCCIO on line 714 and the pad 750, and provides that voltage as a bias to the well of devices M1 710 and M3 730. In this way, as the pad voltage exceeds the voltage VCCIO on line 714, the well of device M1 710 is biased such that the voltage across the drain-to-well diode M1 710 is near zero"

Examiner's assertion that output noise and power consumption provide motivations to combine Fugate with Miyanaga and Lin is incorrect. Furthermore, as described above, the bulk terminals of transistors (4) of Miyanaga and P1 of Lin appear to be connected to a fixed supply voltage. In other words, forward biasing of the drain-to-bulk regions do not appear to be of concern to either Miyagnaga or Lin. Therefore, contrary to the Examiner's assertions, the requisite motivation to combine Fugate with Miyanaga and Lin is lacking. Claim 36 and its dependent claims 37-38 are thus allowable over Miyanaga in view of Toyoshima, Lin and Fugate for at least the reasons cited above. Claims 39-41 are likewise allowable for at least the same reasons as is claim 36.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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